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EXAMINER	
NGUYEN, THINH T	

ART UNIT	PAPER NUMBER
2818	

MAIL DATE	DELIVERY MODE
07/12/2010	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/581,755	HE ET AL.	
	Examiner	Art Unit	
	THINH T. NGUYEN	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 April 2010*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9 and 18-32* is/are pending in the application.

4a) Of the above claim(s) *18-24* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9 and 25-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This is in response to Applicant's Amendment filed April 20th 2010

Note that the figures and reference numbers referred to in this Office Action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Claims 1-9, 18-32 are pending in the Application with claims 18-24 withdrawn from consideration as directed to non-elected claims.

2. Applicant's amendments to independent claims 1, 29 and claims 4,6,9,27,28, 31 have necessitated new grounds of rejection for claims 1-9, 18-32. See MPEP § 706.07(a).

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in-
(1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or

(2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United

States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

4. Claims 1, 4, 7 are rejected under 35 U.S.C. §102(e) as being anticipated by Zhu et al. (U.S. Patent 7,217,994) thereafter Zhu 994.

With regard to claim 1, Zhu 994 discloses (the abstract,fig 2,fig4) a microelectronic device comprising:

a package substrate having a first side and an opposing second side;(element # 16, fig 2,fig4) a package connector at the second side of the package substrate and a board coupled to the package connector;(fig 2 fig 4, element #12) a microprocessor adjacent to the first side of the package substrate; (fig 2,fig 4 chip 14) and a memory device adjacent to the second side of the package substrate (fig 2, elements #42,#44, fig 4,elements # 52,54,column 3 lines 40-55,column 4 lines 15-35) wherein the package substrate is electrically coupled to at least one of the microprocessor and the memory device and wherein the memory device is located in a cavity (claim 1 ,fig 2,fig 4) defined by the package connector, the package substrate, and the board..

Note that Zhu 994 discloses that chip 14 is an ASIC (Application Specific processor) but it can also be a regular microprocessor; see Zhu 994 column 2 lines 10-30)

With regard to claim 4 , Zhu 994 discloses (fig 2, fig 4) a microelectronic device wherein the memory device is disposed on a land side of the substrate (note that Zhu 994 discloses a substrate (inherent to fig 2 ,fig 4, element # 16 that has land side conductive pads and conductive traces on top)

Fig. 2

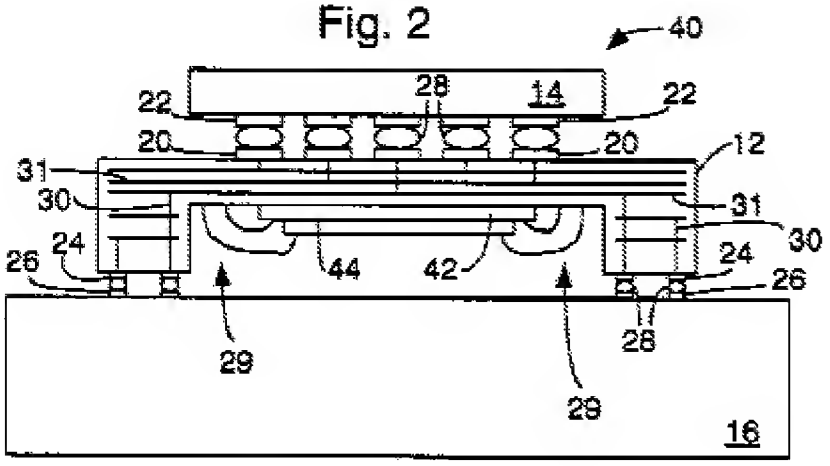
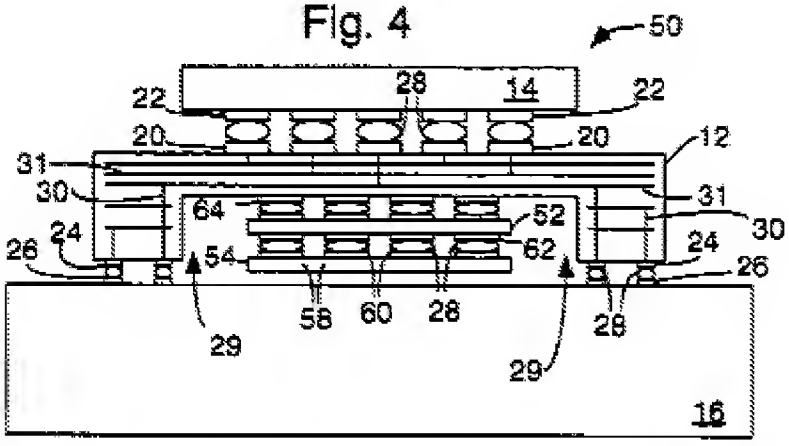


Fig. 4



ZHU 994 DISCLOSURES

With regard to claim 7, Zhu 994 (the abstract, fig 2, fig 4) discloses a microelectronic device further comprising a die including one selected from the group including a memory device, a memory controller, an application specific integrated circuit (ASIC), a graphics processor, a signal processor, a radio transceiver, and a combination thereof.(not that Zhu discloses that his microelectronics device can has three chip , one of the chip can be an ASIC or a microprocessor and the other two can be various memory devices (column 2 lines 10-67)

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. §103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 2, 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zhu et al. (U.S. Patent 7,217,994) thereafter Zhu 994.

With regard to claim 2, as set forth in the rejection of claim 1, Zhu 994 discloses all the invention except for the specific wherein the device further has a memory controller electrically coupled to the memory device.

The Examiner, however, take official notice that the incorporation of a memory controller is known in the art at the time the invention was made as evidenced by the disclosure by Ahn (US patent 6, 281,042; column 6 lines 35-50)

A person skilled in the art at the time the invention was made would have been motivated to incorporate a memory controller into the Zhu 994 device in order to enhance its throughput in response to electronics market demands.

With regard to claim 3, as set forth in the rejection of claim 1, Zhu 994 discloses all the invention except for the specific wherein the device further has a thin film capacitor integral to the substrate.

The Examiner, however, take official notice that the incorporation of embedded capacitor in the circuit board is known in the art at the time the invention was made as evidenced by the disclosure of Gilmour et al. (US patent 5,391,917, column 2 lines 25-35)

A person skilled in the art at the time the invention was made would have been motivated to incorporate embedded capacitor into the circuit interposer board of Zhu 994 device in order to enhance the Zhu 994 device integration efficiency.

7. Claims 8,29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zhu et al. (U.S. Patent 7,217,994) thereafter Zhu 994 in view of Klein et al. (US patent Application Publication US 2004/0225821) thereafter Klein 821.

With regard to claim 8, as set forth in the rejection of claim 7, Zhu 994 discloses all the invention including a microelectronic device that has different kind of memory devices (column 4 lines 59-67)

Not specific in Zhu 994 is the limitation wherein the package includes a fourth level cache memory device.

Klein 821, however, discloses a package wherein a fourth level cache memory is included (paragraph [0030]).

It would have been obvious to one of ordinary skill in the art the time the invention was made to incorporate this features, as taught by Klein, into the Zhu 994 device and come up with the invention of claim 8.

The rationale is as the following:

A person skilled in the Art at the time the invention was made would have been motivated to increase the performance of the Zhu 994 device, taught by Klein (paragraph [0034]) in order to improve the capability of the Zhu 994 device and make it a commercial success.

With regard to claim 29, Zhu 994 (the abstract, fig 2,fig 4) discloses all the invention of a microelectronic device comprising: a package substrate; (element # 16, fig 2,fig 4) a package connector coupled to the package substrate (the lower part of element # 12 in fig 2,fig 4) and a board coupled to the package connector;(the upper part of element #12) a microprocessor coupled to the package substrate;(fi2,fig 4 element # 14) and a memory device coupled to the package substrate, wherein the memory device is located in a cavity defined by the package connector, the package substrate, and the board. (fig2, fig 4)

Not specific in Zhu 994 disclosure is the limitation wherein the memory device comprises a fourth level cache

Klein 821, however, discloses a package wherein a fourth level cache memory is included (paragraph [0030]).

It would have been obvious to one of ordinary skill in the art the time the invention was made to incorporate this features, as taught by Klein, into the Zhu 994 device and come up with the invention of claim 29.

The rationale is as the following:

A person skilled in the Art at the time the invention was made would have been motivated to increase the performance of the Zhu 994 device, taught by Klein 821 (paragraph [0034]) in order to improve the capability of the Zhu 994 device and make it a commercial success.

With regard to claims 25, 30, as set forth in the rejection of claim 8, 29; Zhu 994 discloses all the invention except for the limitation as recited in claims 25, 30.

These limitations, however, are considered obvious for the following rationale:

The selection of parameters such as **energy, concentration, temperature, time, molar fraction, depth, thickness, etc.,** would have been obvious and involve routine optimization which has been held to be within the level of ordinary skill in the art. "Normally, it is to be expected that a change in **energy, concentration, temperature, time, molar fraction, depth, thickness, etc.,** or in combination of the parameters would be an unpatentable modification. Under some circumstances, however, changes such as these may impart patentability to a process if the particular ranges claimed produce a new and unexpected result which is different in kind and not merely degree from the results of the prior art ... such ranges are termed "critical ranges and the applicant has the burden of proving such criticality.... More particularly, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." *In re Aller 105 USPQ233, 255 (CCPA 1955). See*

*also In re Waite 77 USPQ 586 (CCPA 1948); In re Scherl 70 USPQ 204 (CCPA 1946); In re Irmscher 66 USPQ 314 (CCPA 1945); In re Norman 66 USPQ 308 (CCPA 1945); In re Swenson 56 USPQ 372 (CCPA 1942); In re Sola 25 USPQ 433 (CCPA **1935);** In re Dreyfus 24 USPQ 52 (CCPA **1934).***

With regard to claim 26, the limitation as recited in claim 26 is inherent to cache memory in micro processing device disclosed by Zhu 994 in view of Klein 821 (i.e. using a smaller capacity memory with faster speed to interface a larger capacity memory that has slower speed with the central processing unit to make the efficient use of system memory and increase throughput)

With regard to claim 31, Klein disclosed a third level cache (paragraph [0003], moreover, the limitation as recited in claim 31 is inherent to cache memory in micro processing device disclosed by Zhu 994 in view of Klein 821 (i.e. using a smaller capacity memory with faster speed to interface a larger capacity memory that has slower speed with the central processing unit to make the efficient use of system memory)

With regard to claim 27, 28, 32; the use of Land grid array and Pin Grid Array are technologies known by a person skilled in the art at the time the invention was made equivalent to the Ball grid array disclosed by Zhu 994 (fig 2, fig 4)

8. Claims 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Zhu et al. (U.S. Patent 7,217,994) thereafter Zhu 994 in view of Ahn et al. (US patent 6,281,042) thereafter Ahn 042.

With regard to claim 9, as set forth in the rejection of claim 1, Zhu 994 discloses all the invention except for the use of a head spreader thermally coupled to one or more of the die. Ahn 042, however, disclosed a multichip module that has a heat spreader thermally coupled to one or more of the die (column 5 lines 30-36)

8. Claims 1-9, 25-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (the AAPA in fig 2, paragraph [0009] in the present Application Specification.) in view of Gilmour et al. (US patent 5,391,917) thereafter Gilmour 917

With regard to claim 1, the AAPA (fig 2 of the present application) disclosed all the invention of claim 1 including a package substrate (fig 2 # 214) having a first side and an opposing second side; a package connector at the second side of the package substrate (fig 2 # 210) and a board (fig 2 #208) coupled to the package connector) a microprocessor (fig 2 #206 , paragraph [0009] of the present Application Specification) adjacent to the first side of the package substrate; and a cavity defined by the package connector, the package substrate, and the board..(fig 2 of the present Application)

Not disclosed in the AAPA is the limitations wherein the package has a memory device adjacent to the second side of the package substrate wherein the package substrate is electrically coupled to at least one of the microprocessor and the memory device and wherein the memory device is located in the cavity defined by the package connector, the package substrate, and the board..

Gilmour 917, however, discloses a multichip module microelectronic device wherein memory devices are located on the opposite side of microprocessor devices

It would have been obvious to one of ordinary skill in the art the time the invention was made to incorporate this features, as taught by Gilmour 917, into the AAPA and come up with the invention of claim 1.

The rationale is as the following:

A person skilled in the Art at the time the invention was made would have been motivated to increase the functionality of the AAPA device, taught by Gilmour 917 (the abstract, column 3 lines 1-20) in order to improve the versatility and capability of the AAPA device and make it a commercial success.

Note that the modification using the Gilmore 917 disclosures can be easily realized in fig 2 of the AAPA by putting the memory devices on the opposite side of the board similar to the capacitors inside the cavity of the AAPA device in fig 2.

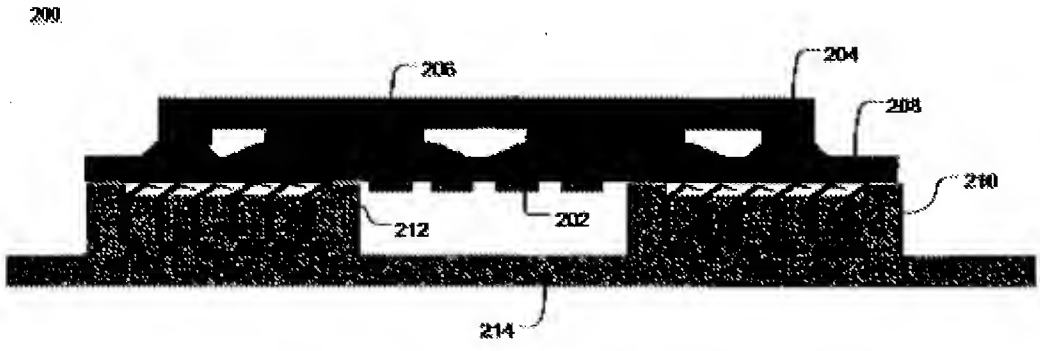


FIG. 2
Prior Art

With regard to claim 29 , as set forth in the rejection of claim 1, the combined AAPA in view of Gilmour 917 discloses all the invention of a microelectronic device comprising: a package substrate; a package connector coupled to the package substrate and a board coupled to the package connector; a microprocessor coupled to the package substrate; and a memory device coupled to the package substrate, and wherein the memory device is located in a cavity defined by the package connector, the package substrate, and the board. Except for the limitation wherein the memory device comprises a fourth level cache

This limitation, however, is s considered obvious because the increasing the level of cache memory allow slower low cost small size memory element physically separate from the microprocessor to increase the speed and the throughput of the system is known in the art at the time the invention was made.(see the disclosure by Klein et al US patent Application Publication US 2004/0225821)

With regard to claim 2, Gilmore 917 disclosed the incorporation of the cross point switching devices S1 to Sj (in fig 11) into the package that perform the function of a memory controller (column 7 lines 9-55)

With regard to claim 3, Gilmour 917 discloses a device that has a thin film capacitor integral to the substrate (column 2 lines 25-35).

With regard to claim 4, the combined AAPA in view of Gilmore 917 disclosed a microelectronic device wherein the memory device is disposed on a land side of the package substrate (the AAPA fig 2 of the present Application)

With regard to claim 5, Gilmour 917 discloses (fig 8, fig 10,fig 11) a microelectronic device further comprising a third die including a second microprocessor, a fourth die including a third microprocessor, and a fifth die including a fourth microprocessor.

With regard to claim 6, Gilmour 917 discloses (fig 8, fig 10, fig 11) a memory device electrically coupled by one selected from the group including a wire bond electrical interconnect, a flip-chip ball grid array electrical interconnect, a lead frame interconnect, and a combination thereof.

With regard to claim 7, Gilmour 917 discloses (fig 7,fig 9,fig 10,fig 11) a microelectronic device further comprising a die including one selected from the group including a memory device, a memory controller, an application specific integrated circuit (ASIC), a graphics processor, a signal processor, a radio transceiver, and a combination thereof.(column 7 lines 54-60)

With regard to claim 8, as set forth in the rejection of claim 7, the combined AAPA in view of Gilmour 917 device discloses all the invention including a cache die (Gilmour 917 fig 10, chip 61, column 7 lines 1-9). except for the inclusion of a fourth level cache memory.

This limitation, however, is s considered obvious because the increasing the level of cache memory allow slower low cost small size memory element physically separate from the microprocessor to increase the speed and the throughput of the system is known in the art at the time the invention was made (see the disclosure by Klein et al US patent Application Publication US 2004/0225821)

With regard to claim 9, the AAPA (fig 2 of the present Application) discloses the use of a head spreader (fig 2, # 204, paragraph [0009] of the specification of the present Application)

With regard to claim 26, the limitations as recited in claim 26, is inherent characteristics to cache memory in micro processing device disclosed by the AAPA in view of Gilmour (i.e. using a smaller capacity memory with faster speed to interface a larger capacity memory that has slower speed with the central processing unit to make the efficient use of system memory and increase throughput)

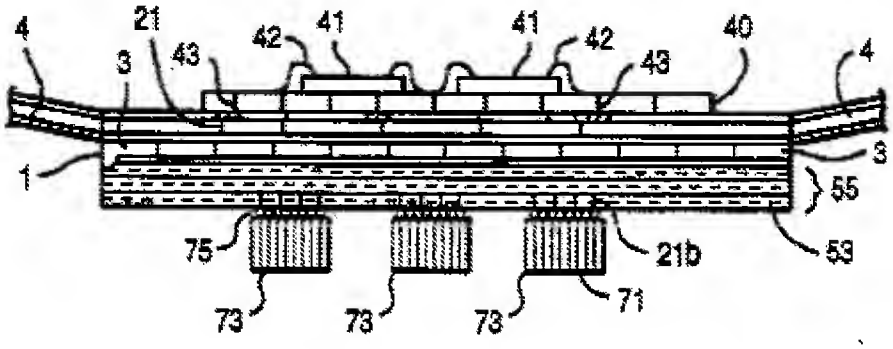


FIG. 7

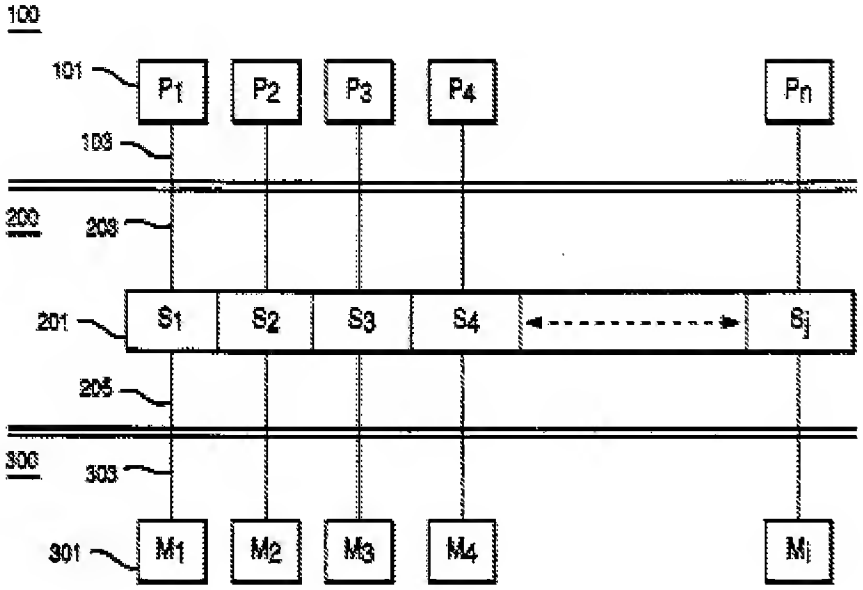


FIG. 11

GILMOUR 917 DISCLOSURES

With regard to claims 25, 30, as set forth in the rejection of claim 8, 29; the combined AAPA in view of Gilmour 917 discloses all the invention except for the limitation as recited in claims 25, 30.

These limitations, however, are considered obvious for the following rationale:

The selection of parameters such as **energy, concentration, temperature, time, molar fraction, depth, thickness, etc.,** would have been obvious and involve routine optimization which has been held to be within the level of ordinary skill in the art. "Normally, it is to be expected

that a change in **energy, concentration, temperature, time, molar fraction, depth, thickness, etc.,** or in combination of the parameters would be an unpatentable modification. Under some circumstances, however, changes such as these may impart patentability to a process if the particular ranges claimed produce a new and unexpected result which is different in kind and not merely degree from the results of the prior art ... such ranges are termed "critical ranges and the applicant has the burden of proving such criticality.... More particularly, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." *In re Aller 105 USPQ233, 255 (CCPA 1955). See also In re Waite 77 USPQ 586 (CCPA 1948); In re Scherl 70 USPQ 204 (CCPA 1946); In re Irmscher 66 USPQ 314 (CCPA 1945); In re Norman 66 USPQ 308 (CCPA 1945); In re Swenson 56 USPQ 372 (CCPA 1942); In re Sola 25 USPQ 433 (CCPA **1935);** In re Dreyfus 24 USPQ 52 (CCPA **1934).***

With regard to claim 31, as set forth in the rejection of claim 29, the AAPA in view Gilmour 917 device discloses all the invention except for a third level cache with speed faster than system memory bus and the capacity of the fourth level cache.

This limitation however, is considered obvious because the use of Level three cache is known in the art at the time the invention was made. A person skilled in the art at the time would have been motivated to use a third level cache in combination with a fourth level cache to increase the processing speed of the AAPA in view of Gilmour 917 device. Furthermore, the limitation wherein a third level cache with speed faster than system memory bus and the capacity of the fourth level cache is inherent to cache memory hierarchy of the system memory in micro processing device.

With regard to claim 27, 28, 32; the use of Land grid array and Pin Grid Array are technologies known by a person skilled in the art at the time the invention was made equivalent to the Ball grid array disclosed by the AAPA in view of Gilmour 917 device

CONCLUSION

9. **THIS ACTION IS MADE FINAL. Applicant's amendments to independent claims 1, 29 and claims 4,6,9,27,28, 31 have necessitated new grounds of rejection for claims 1-9, 18-32 and therefore this Action is made FINAL** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thinh T Nguyen whose telephone number is 571-272-1790. The

examiner can normally be reached on 9:30 am - 6:30 pm Monday to Friday. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, STEVEN LOKE can be reached on 571-272-1657. The fax phone numbers for the organization where this application or proceeding is assigned is 571-273-8300

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval [PAIR] system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Thinh T Nguyen/

Primary Examiner

Art Unit 2818